TSMC-01-1300

April 15, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/772,940 02/05/04

Kuan-Lun Chang et al.

A METHOD OF FORMING A SHALLOW TRENCH - DEEP TRENCH ISOLATION REGION FOR A BiCMOS/CMOS TECHNOLOGY

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 26, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 4/26/04

U.S. Patent 6,214,696 to Wu, "Method of Fabricating Deep-Shallow Trench Isolation," discloses a semiconductor manufacturing process to fabricate a trench isolation.

U.S. Patent 5,895,253 to Akram, "Trench Isolation for CMOS Devices," discusses an isolation trench with an insulator, and a method of forming the same using self-aligned processsing techniques.

U.S. Patent 6,232,043 to Lin et al., "Rule to Determine CMP Polish Time," discloses a simple method for calculating the optimum amount of HDP deposited material that needs to be removed during CMP (without introducing dishing).

U.S. Patent 6,194,287 to Jang, "Shallow Trench Isolation (STI) Method with Reproducible Alignment Registration," discloses a method for retaining of alignment marks upon a microelectronics substrate when filling trenches formed within the substrate.

U.S. Patent 6,255,184 to Sune, "Fabrication Process for a Three Dimensional Trench Emitter Bipolar Transistor," discloses a method used to fabricate a bipolar transistor device, featuring a three dimensional trench emitter region.

U.S. Patent 6,110,794 to Liu, "Semiconductor Having Self-Aligned, Buried Etch Stop for Trench and Manufacture Thereof," discloses a semiconductor fabrication process which uses a buried, oxygen-rich layer as a stop etch in a trench isolation area, with minimal masking.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Sheet 1 of 1

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

APR 2 9 2004 PATENT & TRADEMARK OFFICE

Docket Number (Optional)	Application Number
TSMC-01-1300	10/772,940
Applicant: Kuan-Lun Chang et al.	
Filing Date: 02/05/04	Group Art Unit

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6214696	4/10/01	Wu	438	424	9/10/99
	5895253	4/20/99	Akram	438	424	8/22/97
	6232043	5/15/01	Lin et al.	430	317	5/25/99
	6194287	2/27/01	Jang	438	427	4/2/99
	6255184	7/3/01	Sume	438	337	8/30/99
	6110794	8/29/00	Lin	438	407	8/19/98

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant